

Amendments to the Claims:

Please amend claims 5, 6, 8, 10, 11, and 12 as follows.

This listing of claims replaces all prior versions, and listings, of claims in the application.

Listing of claims:

1. (Original) A memory device comprising:  
first memory cells connected to a bit line;  
second memory cells connected to a complementary bit line;  
a bit-line equalization circuit which pre-charges the bit line and the complementary bit line to a power source voltage level;  
a sensing enable unit which changes the voltage at its output node to a ground voltage level in response to a sensing enable signal; and  
a bit-line sense amplifier in which when the first memory cells connected to the bit line are selected, a second addressing signal for selecting the second memory cells connected to the complementary bit line is generated with a voltage level higher than that of a first addressing signal for selecting the first memory cells connected to the bit line, thereby amplifying a voltage level of the bit line and a voltage level of the complementary bit line using a first current path and a second current path,  
wherein the first current path is formed between the output node of the sensing enable unit and the bit line in response to the voltage level of the complementary bit line and the first addressing signal, and the second current path is formed between the output node of the sensing enable unit and the complementary bit line in response to the voltage level of the bit line and the second addressing signal.
2. (Original) The memory device according to claim 1, wherein when the second memory cells connected to the complementary bit line are selected, the first addressing signal is generated with a voltage level higher than that of the second addressing signal, thereby amplifying the

voltage level of the bit line and the voltage level of the complementary bit line using the first current path and the second current path.

3. (Original) The memory device according to claim 1, wherein the sensing enable unit is an inverter comprising a PMOS transistor and an NMOS transistor connected in series between the power source voltage and the ground voltage, the gates of the PMOS and NMOS transistors being supplied with the sensing enable signal.

4. (Previously Presented) The memory device according to claim 1, wherein the bit-line sense amplifier comprises:

a first PMOS transistor the source of which is supplied with the power source voltage, the drain of which is connected to the bit line, and the gate of which is connected to the complementary bit line;

a second PMOS transistor the source of which is supplied with the power source voltage, the drain of which is connected to the complementary bit line, and the gate of which is connected to the bit line;

first and second NMOS transistors connected in series between the bit line and the output node of the sensing enable unit, the gate of the first NMOS transistor being supplied with a first control signal which is activated when the memory cells connected to the complementary bit line are selected, the gate of the second NMOS transistor being connected to the complementary bit line; and

third and fourth NMOS transistors connected in series between the complementary bit line and the output node of the sensing enable unit, the gate of the third NMOS transistor being supplied with a second control signal which is activated when the memory cells connected to the bit line are selected, the gate of the fourth NMOS transistor being connected to the bit line.

5. (Currently Amended) The memory device according to claim ~~[[1]]~~4, wherein the first control signal is generated from a first control signal generating circuit, and the first control signal generating circuit comprises:

a ~~first~~ third PMOS transistor the source of which is supplied with a first source voltage having a voltage level higher than a second source voltage, and the gate of which is supplied with an inverted signal of the second addressing signal;

a ~~second~~ fourth PMOS transistor the source of which is supplied with the second source voltage, and the gate of which is supplied with the first addressing signal; and

[[an]]a fifth NMOS transistor the source of which is supplied with the ground voltage, the gate of which is supplied with the sensing enable signal, and the drain of which is connected to the drains of the ~~first and second~~ third and fourth PMOS transistors.

6. (Currently Amended) The memory device according to claim [[1]]4, wherein the second control signal is generated from a second control signal generating circuit, and the second control signal generating circuit comprises:

a ~~first~~ third PMOS transistor the source of which is supplied with the first source voltage having a voltage level higher than a second source voltage, and the gate of which is supplied with the second addressing signal;

a ~~second~~ fourth PMOS transistor the source of which is supplied with the second source voltage, and the gate of which is supplied with an inverted signal of the first addressing signal; and

[[an]]fifth NMOS transistor the source of which is supplied with the ground voltage, the gate of which is supplied with the sensing enable signal, and the drain of which is connected to the drains of the ~~first and second~~ third and fourth PMOS transistors.

7. (Original) A memory device comprising:

first memory cells connected to a bit line;

second memory cells connected to a complementary bit line;

a bit-line equalization circuit which pre-charges the bit line and the complementary bit line to a ground voltage level;

a sensing enable unit which changes the voltage at its output node to a power source voltage level in response to a sensing enable signal; and

a bit-line sense amplifier in which when the first memory cells connected to the bit line are selected, a second addressing signal for selecting the second memory cells connected to the complementary bit line is generated with a voltage level lower than that of a first addressing signal for selecting the first memory cells connected to the bit line, thereby amplifying a voltage level of the bit line and a voltage level of the complementary bit line using a first current path and a second current path,

wherein the first current path is formed between the output node of the sensing enable unit and the bit line in response to the voltage level of the complementary bit line and the first addressing signal, and the second current path is formed between the output node of the sensing enable unit and the complementary bit line in response to the voltage level of the bit line and the second addressing signal.

8. (Currently Amended) The memory device according to claim [[6]]7, wherein when the second memory cells connected to the complementary bit line are selected, the first addressing signal is generated with a voltage level lower than that of the second addressing signal, thereby amplifying the voltage level of the bit line and the voltage level of the complementary bit line using the first current path and the second current path.

9. (Original) The memory device according to claim 7, wherein the sensing enable unit is an inverter comprising a PMOS transistor and an NMOS transistor connected in series between the power source voltage and the ground voltage, the gates of the PMOS and NMOS transistors being supplied with the sensing enable signal.

10. (Currently Amended) The memory device according to claim 7, wherein the bit-line sense amplifier comprises:

a first NMOS transistor the source of which is supplied with the ground voltage, the drain of which is connected to the bit line, and the gate of which is connected to the complementary bit line;

a second NMOS transistor the source of which is supplied with the ~~power source~~ ground

voltage, the drain of which is connected to the complementary bit line, and the gate of which is connected to the bit line;

first and second PMOS transistors connected in series between the bit line and the output node of the sensing enable unit, the gate of the first PMOS transistor being supplied with a first control signal which is activated when the memory cells connected to the complementary bit line are selected, the gate of the second PMOS transistor being connected to the complementary bit line; and

third and fourth PMOS transistors connected in series between the complementary bit line and the output node of the sensing enable unit, the gate of the third PMOS transistor being supplied with a second control signal which is activated when the memory cells connected to the bit line are selected, the gate of the fourth PMOS transistor being connected to the bit line.

11. (Currently Amended) The memory device according to claim ~~[[7]]~~10, wherein the first control signal is generated from a first control signal generating circuit, and the first control signal generating circuit comprises:

a ~~first~~ third NMOS transistor the source of which is supplied with a second ground voltage having a voltage level lower than a first ground voltage, and the gate of which is supplied with the second addressing signal;

a ~~second~~ fourth NMOS transistor the source of which is supplied with the first ground voltage, and the gate of which is supplied with the inverted first addressing signal; and

a fifth PMOS transistor the source of which is supplied with the power source voltage, the gate of which is supplied with the inverted sensing enable signal, and the drain of which is connected to the drains of the ~~first and second~~ third and fourth NMOS transistors.

12. (Currently Amended) The memory device according to claim ~~[[7]]~~10, wherein the second control signal is generated from a second control signal generating circuit, and the second control signal generating circuit comprises:

a ~~first~~ third NMOS transistor the source of which is supplied with a second ground voltage having a voltage level lower than a first ground voltage, and the gate of which is supplied

with the second addressing signal;

a ~~second~~ fourth NMOS transistor the source of which is supplied with the first ground voltage, and the gate of which is supplied with an inverted signal of the first addressing signal; and

a fifth PMOS transistor the source of which is supplied with the power source voltage, the gate of which is supplied with the inverted sensing enable signal, and the drain of which is connected to the drains of the ~~first and second~~ third and fourth NMOS transistors.

13. (Original) A method of amplifying voltage levels of a bit line and a complementary bit line of a memory device, the method comprising steps of:

(a) pre-charging the bit line and the complementary bit line to a power source voltage level;

(b) enabling first memory cells connected to the bit line to transfer data of the first memory cells to the bit line; and

(c) allowing an output node of a sensing enable unit to have a ground voltage level in response to a sensing enable signal,

wherein step (b) comprises:

(b-1) generating a second addressing signal for selecting the second memory cells connected to the complementary bit line with a voltage level higher than that of a first addressing signal for selecting the first memory cells; and

(b-2) amplifying the voltage level of the bit line and the voltage level of the complementary bit line using a first current path and a second current path, the first current path being formed between the output node of the sensing enable unit and the bit line in response to the voltage level of the complementary bit line and the first addressing signal, the second current path being formed between the output node of the sensing enable unit and the complementary bit line in response to the voltage level of the bit line and the second addressing signal.

14. (Original) The method according to claim 13, further comprising (d) enabling second memory cells connected to the complementary bit line to transfer data of the second memory cells to the complementary bit line,

wherein step (d) comprises:

(d-1) generating the first addressing signal with a voltage level higher than that of the second addressing signal; and

(d-2) amplifying the voltage level of the bit line and the voltage level of the complementary bit line by using the first current path and the second current path.

15. (Original) A method of amplifying voltage levels of a bit line and a complementary bit line of a memory device, the method comprising:

(a) pre-charging the bit line and the complementary bit line to a ground voltage level;

(b) enabling first memory cells connected to the bit line to transfer data of the first memory cells to the bit line; and

(c) allowing an output node of a sensing enable unit to have a power source voltage level in response to a sensing enable signal,

wherein step (b) comprises:

(b-1) generating a second addressing signal for selecting the second memory cells connected to the complementary bit line with a voltage level lower than that of a first addressing signal for selecting the first memory cells; and

(b-2) amplifying the voltage level of the bit line and the voltage level of the complementary bit line using a first current path and a second current path, the first current path being formed between the output node of the sensing enable unit and the bit line in response to the voltage level of the complementary bit line and the first addressing signal, the second current path being formed between the output node of the sensing enable unit and the complementary bit line in response to the voltage level of the bit line and the second addressing signal.

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16. (Original) The method according to claim 15, further comprising (d) enabling second memory cells connected to the complementary bit line to transfer data of the second memory cells to the complementary bit line,

wherein step (d) comprises:

(d-1) generating the first addressing signal with a voltage level lower than that of the second addressing signal; and

(d-2) amplifying the voltage level of the bit line and the voltage level of the complementary bit line by using the first current path and the second current path.